ABSTRACT OF THE DISCLOSURE

Upon a triggering event, a delay chain shifts data out at a higher rate than incoming packets and a processor controls bypassing circuitry to reduce the latency of hardware implementations of, for example, 802.11a OFDM receivers, with long delay

5   chains. The signal processing algorithms used to recover symbol timing need a large number of samples stored in a delay chain, often consisting of pipelined registers. Such a delay chain introduces a large lag between the time samples have been acquired by the data converters and the time they are processed. This delay makes it difficult for higher level network layer implementations to meet the deadlines of 802.11a WLAN protocol.

10   The proposed scheme implements dynamic reduction in the depth of the delay chain once timing recovery has been performed. A multi-step scheme achieves exponential reduction in the number of elements in the delay chain in every step.